OIPE JC19 JAN 19 2005 PATENT & TRADEMARK OFFICE

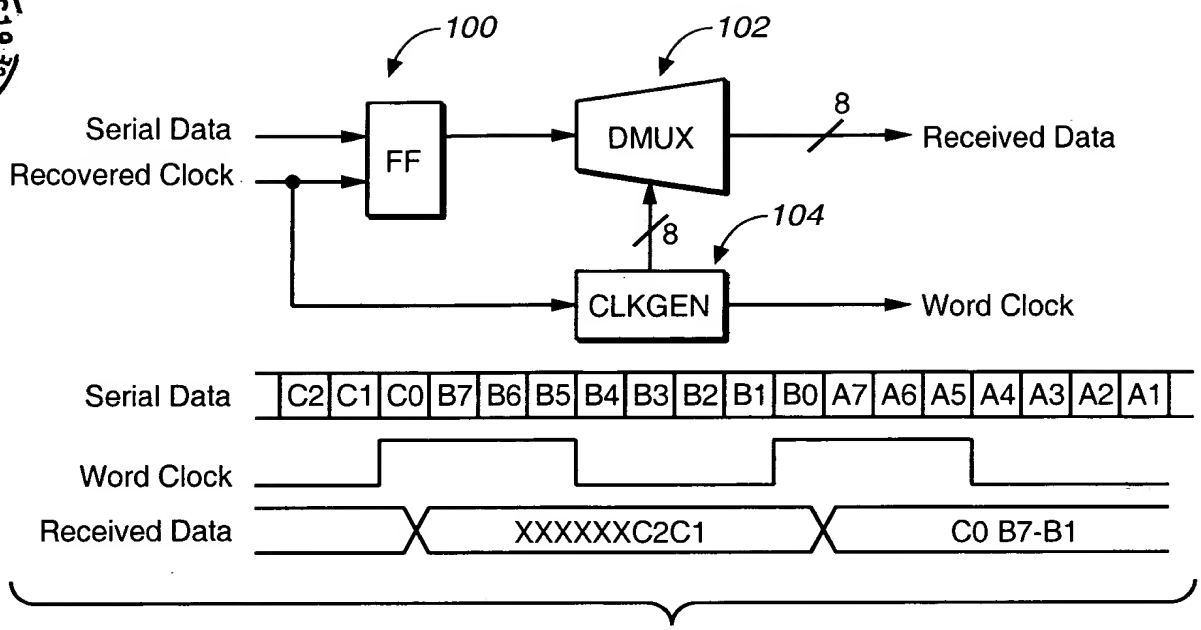

FIG._1
(PRIOR ART)

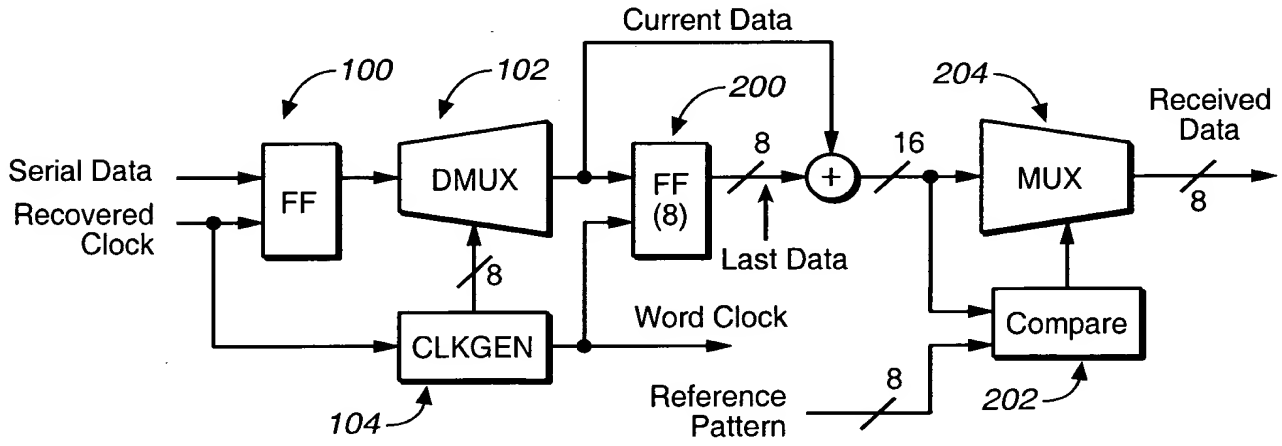

FIG._2
(PRIOR ART)

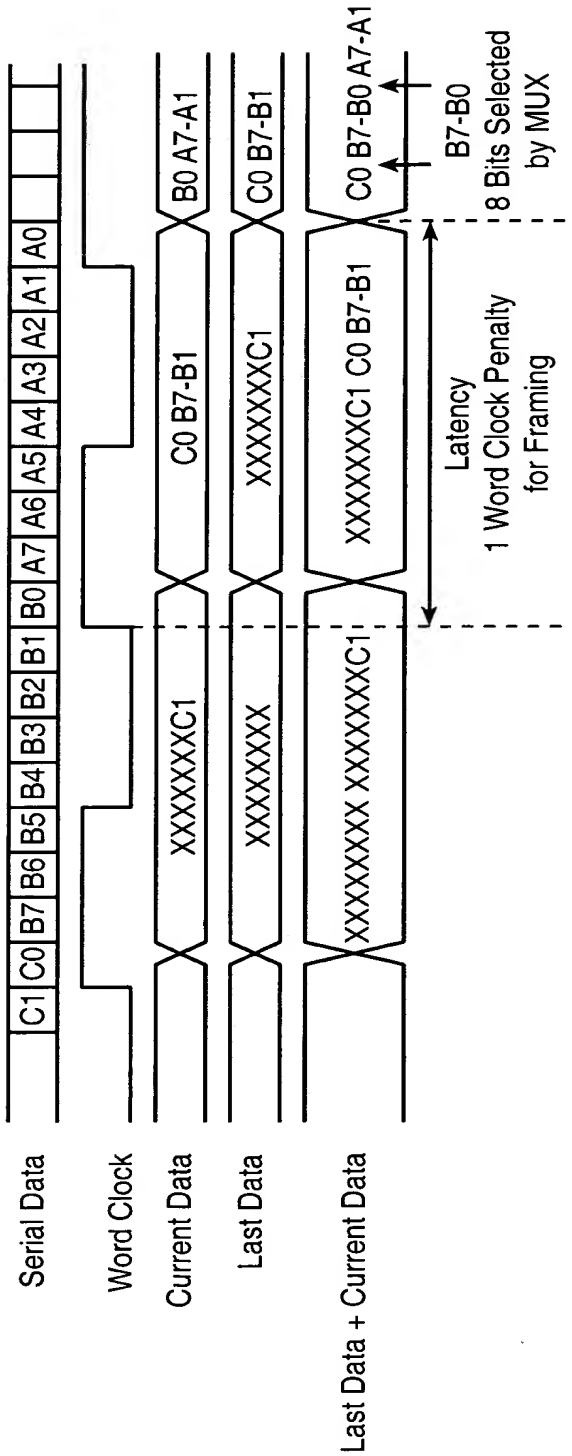

FIG._3
(PRIOR ART)

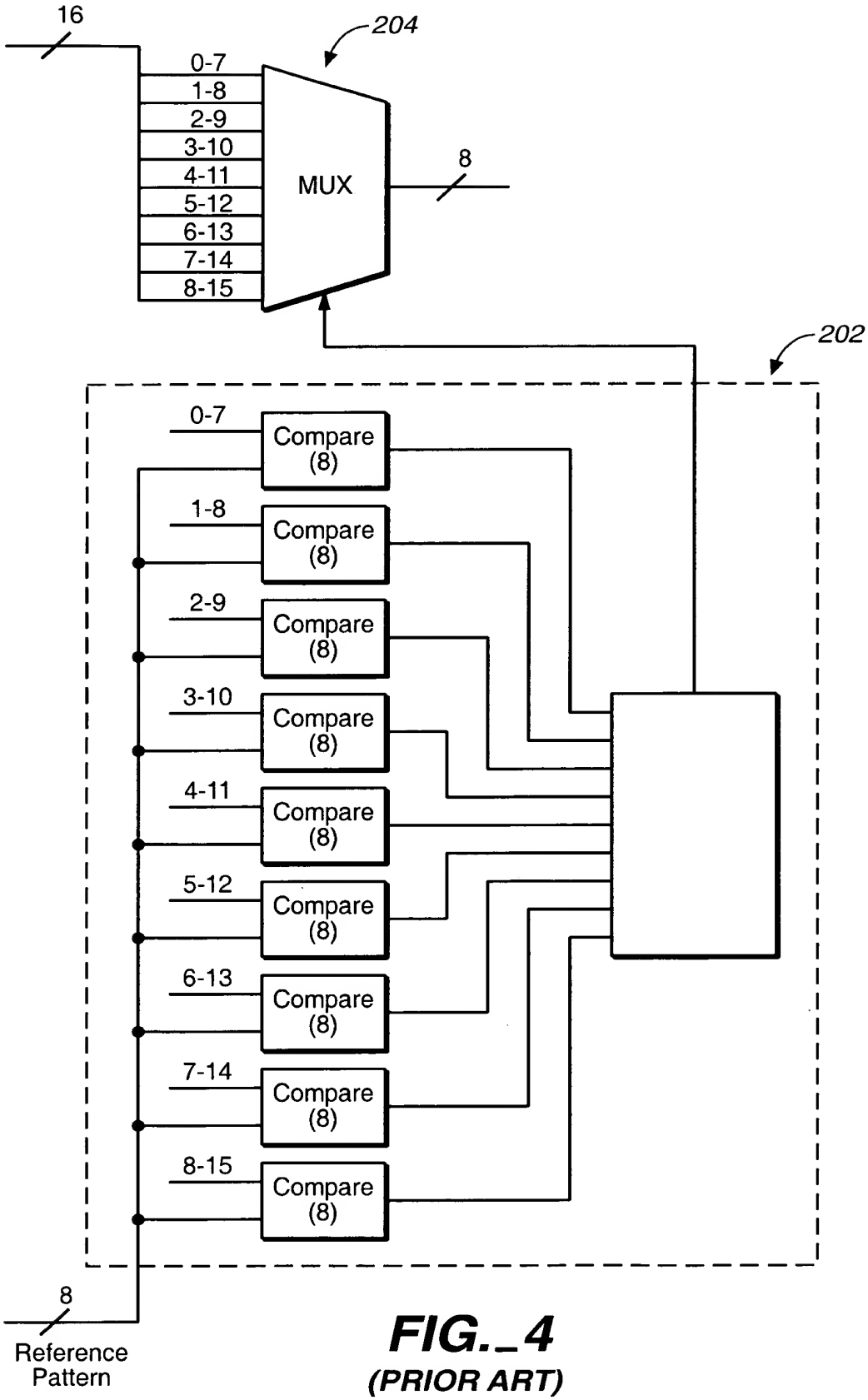

FIG._4
(PRIOR ART)

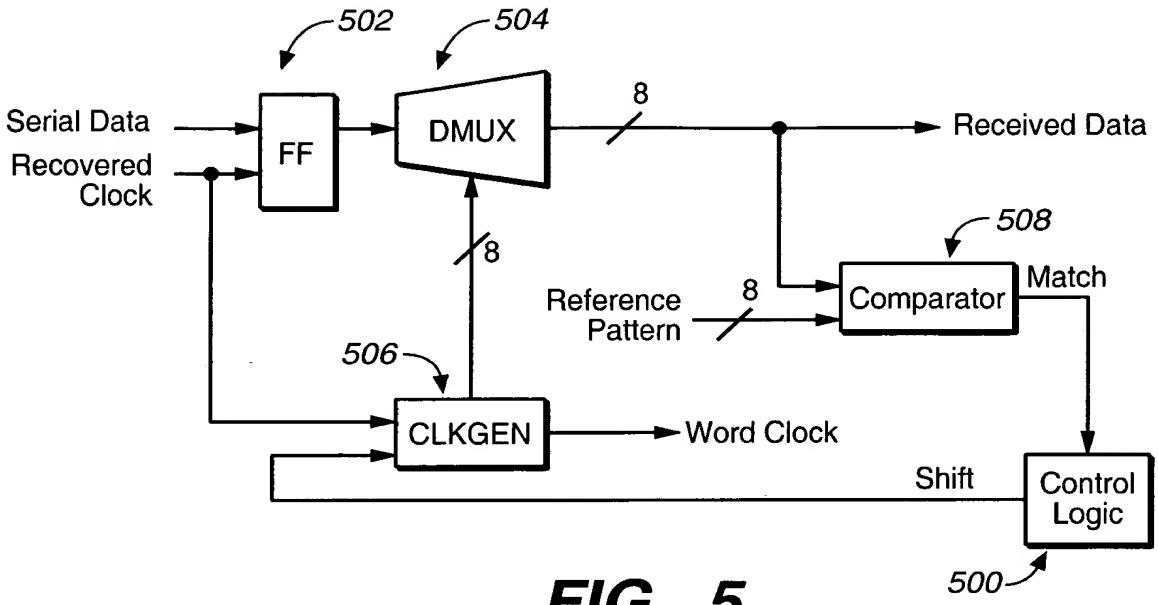
502
504
Serial Data
Recovered Clock
FF
DMUX
8
Received Data
508
8
Reference Pattern
8
Comparator
Match
506
CLKGEN
Word Clock
Shift
Control Logic
500

FIG._5

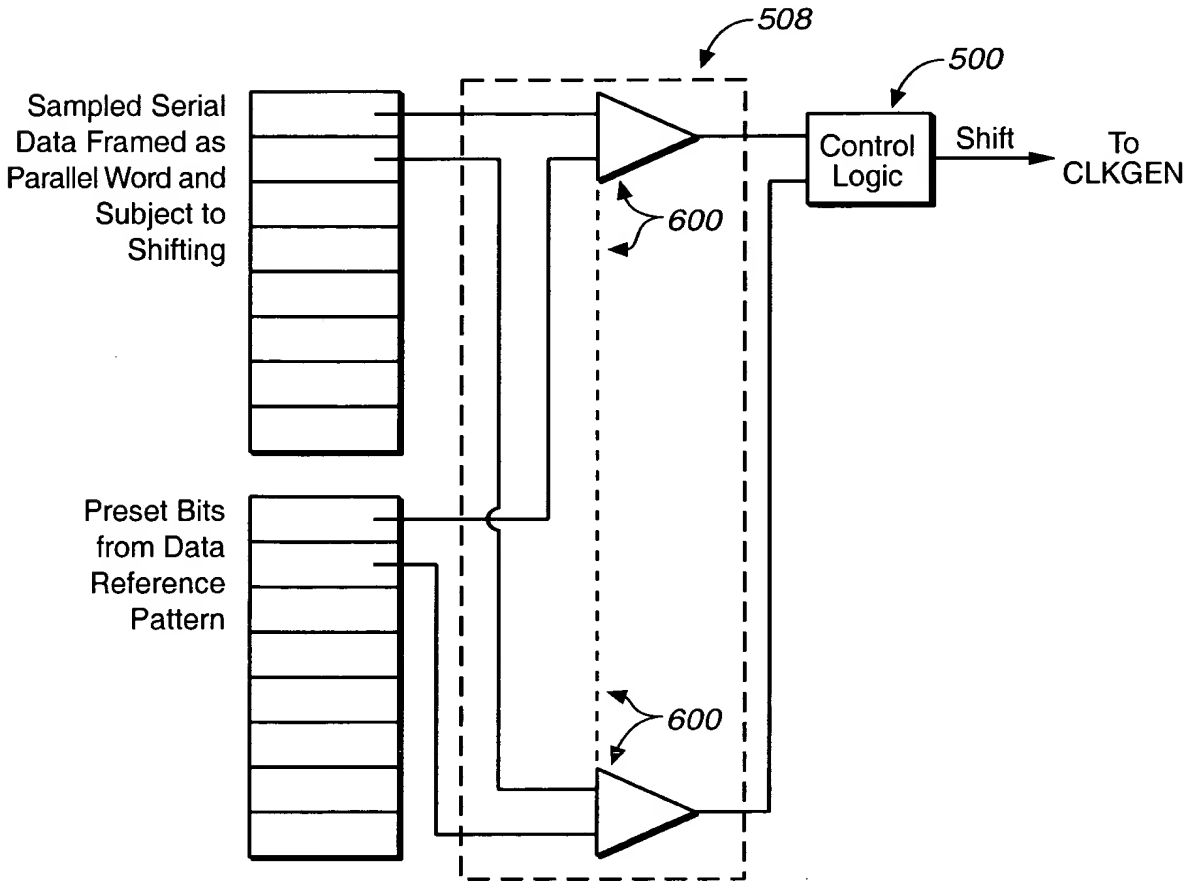
508
500
Sampled Serial Data Framed as Parallel Word and Subject to Shifting
Control Logic
Shift
To CLKGEN
600
Preset Bits from Data Reference Pattern
600

FIG._6

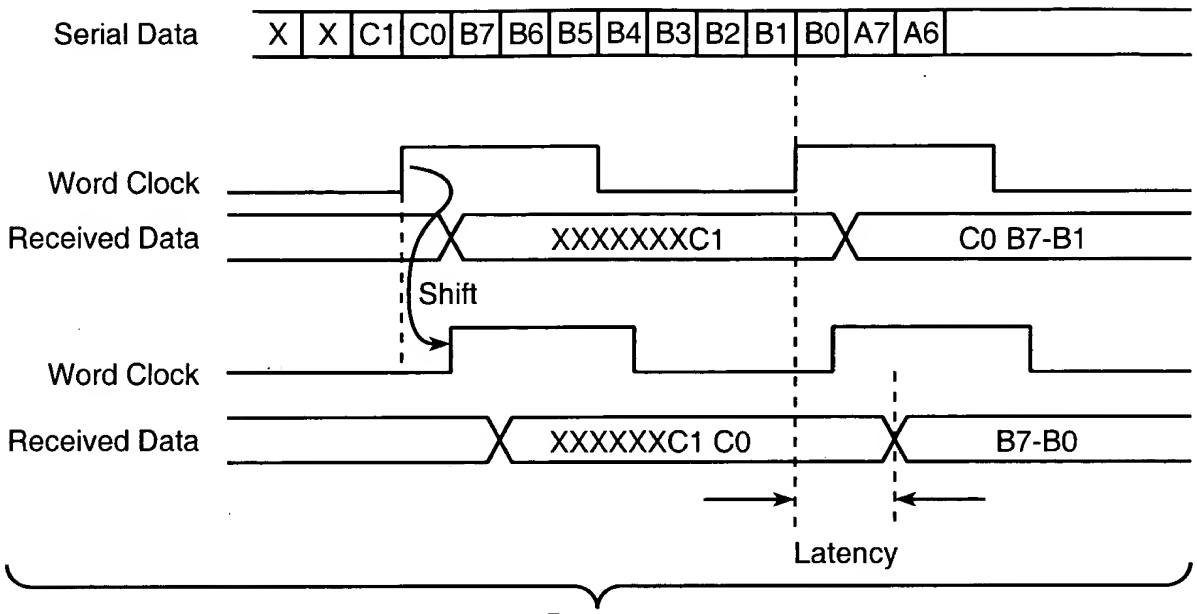
Serial Data
X
X
C1
C0
B7
B6
B5
B4
B3
B2
B1
B0
A7
A6
Word Clock
Received Data
XXXXXXXC1
C0 B7-B1
Shift
Word Clock
Received Data
XXXXXXC1 C0
B7-B0
Latency

FIG._7